Notice of Allowability	Application No.	Applicant(s)	
	10/022,213	SLOBODNIK, RICHARD	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 10/27/2005*.

2. ☒ The allowed claim(s) is/are *1-4 and 8-11*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

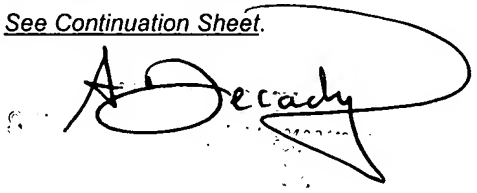
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *See Continuation Sheet*.



Continuation of Attachment(s) 9. Other: IDS is NOT considered because document is not filed on Record.

DETAILED ACTION

1. Claims 1-4 and 8-11 remain pending in this application and have been examined. Claims 1, 4, 8, 9, and 11 have been amended. Claim 7 has been canceled.

2. The rejections of claims 1-4 and 7-11 under 35 U.S.C. 112, 2nd paragraph have been withdrawn by the Examiner because of the Applicant's amendments.

Allowable Subject Matter

Claims 1-4 and 8-11 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to the field of data processing systems. More particularly, this invention relates to the self-testing of memories within data processing systems to detect memory defects.

The claimed invention as set forth in claim 1 (broadest claim) recites features such as: a plurality of different memories, each having a plurality of memory storage locations associated with respective memory addresses, said plurality of different memories having different mappings between physical memory locations and logical addresses associated with said physical memory locations; a self-test controller operable to control self-test of said plurality of different memories including generating physical memory address signals; and a plurality of mapping circuits, each of said plurality of mapping circuits corresponding to a respective one of said plurality of different memories and a plurality of mapping circuits being operable to map said

physical memory address signals generated by said self-test controller to corresponding logical address signals for use by said a respective one of said plurality of different memories to perform a memory test based upon a physical position of said plurality of memory storage locations; and a processor core, wherein said processor core, said plurality of different memories and said self-test controller are formed together on an integrated circuit, and wherein each of said plurality of mapping circuits is part of an interface circuit disposed between said self-test controller and said plurality of different memories said interface circuit being operable to adapt values and timings of signals passed between said self-test controller and said plurality of different memories to accommodate differing value and timing properties of said plurality of different memories.

The prior arts of record teach an electronic device 10 which includes a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (a single memory). The prior arts of record teach also teach a memory address converter 24 (a single mapping circuit) that converts the physical address generated by the BIST engine 20 to a corresponding logical address in the embedded memory 28. The prior arts of record teach further teach a microprocessor (processor core) performs BIST on a memory array having a physical address map distinct from its logical address map; Gold (US-2003/0167428) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, the claimed self-test controller that is adaptable for use with a plurality of different memories

based on generation of a single set of physical memory address signals. Further, a mapping circuit is provided for each of the plurality of different memories which allows the single set of physical memory address signals generated by the self-test controller to be readily adapted and translated to corresponding logical memory address signals appropriate for the particular memory with which the mapping circuit is associated. This provides the novelty such that a single test generated by the self-test controller based on physical memory locations can be translated and applied to a plurality of different memories without requiring a complex self-test controller capable of generating different memory address signals appropriate for the set up and configuration of each of the plurality of different memories under test. In addition, the prior arts of record fail to teach, singly or in combination, that each of the plurality of mapping circuits is part of an interface circuit disposed between the self-test controller and plurality of memories and can adapt values and timings of signals passed between the self-test controller and the plurality of different memories to accommodate the particular properties of those different memories. As such, modification of the prior art of record to include the claimed *self-test controller and plurality of mapping circuits, which is part of an interface circuit* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *self-test controller and plurality of mapping circuits, which is part of an interface circuit* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render

obvious the *self-test controller and plurality of mapping circuits, which is part of an interface circuit* as set forth in claim 1. Independent claim 8 is the method claim of the apparatus claim 1 reciting similar novel limitations as in claim 1 and is allowable for the same reasons as stated above. Hence, claims 1-4 and 8-11 are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefor, the Examiner favors the allowance of claims 1-4 and 8-11. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 12/15/05
Examiner
Art Unit 2138